IN THE CLAIMS:

Please amend the claims as follows. The claims are in the format as required by 35 C.F.R. § 1.121.

1. (Currently Amended) An apparatus for allocating one or more processor resources to an instruction, the apparatus comprising:

a sequence generator that generates one or more resource identifiers using at least a portion of a pseudorandom sequence, each resource identifier corresponding to one of the processor resources; and

a resource identifier selector coupled to the sequence generator, the resource identifier selector selecting one or more of the resource identifiers for allocation to the instruction.

2. (Original) The apparatus as recited in claim 1, wherein the resource identifier selector determines how many resource identifiers, if any, are required by the instruction based on an instruction requirements signal.

3. (Currently Amended) The apparatus as recited in claim 1, further comprising a buffer including two or more buffer entries wherein each processor resource comprises one of the buffer entries.

4. (Original) The apparatus as recited in claim 3, wherein the buffer comprises a reorder buffer.

5. (Original) The apparatus as recited in claim 1, wherein the resource identifier selector further comprises:

one or more comparators coupled to .the resource identifier selection circuit and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison; and

a selector coupled to the one or more comparators and the resource identifier selection circuit.

6. (Original) The apparatus as recited in claim 1, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selection circuit and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison; and

a variable shifter coupled to the one or more comparators and the resource identifier selection circuit.

7. (Original) The apparatus as recited in claim 1, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selection circuit and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison;

a selector coupled to the one or more comparators and the resource identifier selection circuit; and

a highest identifier allocation circuit coupled to the selector.

8. (Original) The apparatus as recited in claim 1, wherein the sequence generator further comprises:

a logic circuit coupled to the resource identifier selector; and

a storage array coupled to the logic circuit and the resource identifier selector.

9. (Original) The apparatus as recited in claim 1, wherein the sequence generator further comprises a storage array coupled to the resource identifier selector.

10. (Original) The apparatus as recited in claim 1, wherein the sequence generator further comprises a logic circuit coupled to the resource identifier selector.

11. (Original) The apparatus as recited in claim 1, further comprising an instruction decode unit and wherein the resource identifier selector generates a decoder stall signal issued to the instruction decode unit.

12. (Original) The apparatus as recited in claim 1, wherein the portion of a pseudorandom sequence comprises a first resource identifier from within the pseudorandom sequence.

13. (Original) The apparatus as recited in claim 12, wherein the resource identifier selection circuit comprises means for generating a second resource identifier from within the pseudorandom sequence based upon the first resource identifier.

14. (Original) The apparatus as recited in claim 1, wherein the sequence generation circuit comprises a storage array and the portion of the pseudorandom sequence comprises a portion of each resource identifier within the pseudorandom sequence stored as elements within the storage array.

15. (Original) The apparatus as recited in claim 14, wherein the portion of each resource identifier within the pseudorandom sequence comprises a least significant bit of each resource identifier within the pseudorandom sequence.

16. (Original) The apparatus as recited in claim 14, wherein the resource identifier selection circuit comprises a variable shifter configured to shift elements of the storage array and the resource identifier selection circuit is configured to index the elements within the storage array.

17. (Original) The apparatus as recited in claim 1, wherein the sequence generation circuit comprises a logic circuit and the portion of a pseudorandom sequence comprises a portion of each resource identifier within the pseudorandom sequence stored as elements within the storage array.

18. (Original) The apparatus as recited in claim 17, wherein the portion of each resource identifier within the pseudorandom sequence comprises a least significant bit of each resource identifier within the pseudorandom sequence.

19. (Original) The apparatus as recited in claim 17, wherein the resource identifier selection circuit comprises a selector and a circuit to determine the highest identifier allocated configured to shift elements of the storage array and the resource identifier selection circuit is configured to index the elements within the storage array.

20. (Currently Amended) A method for allocating one or more processor resources to an instruction, the method comprising the steps of:

generating one or more resource identifiers using at least a portion of a pseudorandom sequence, each resource identifier corresponding to one of the processor resources; and

selecting one or more of the resource identifiers for allocation to the instruction.

21. (Original) The method as recited in claim 20, further comprising the step of determining how many resource identifiers, if any, are required by the instruction based on an instruction requirements signal.

22. (Original) The method as recited in claim 20, further comprising the step of comparing a selected resource identifier to an allocation bound and issuing a control signal in response to the comparison.

23. (Original) The method recited in claim 20, wherein the portion of the pseudorandom sequence comprises a portion of each resource identifier within the pseudorandom sequence stored as elements within a storage array.

24. (Original) The method as recited in claim 23, wherein the portion of each resource identifier within the pseudorandom sequence comprises a least significant bit of each resource identifier within the pseudorandom sequence.

25. (Original) The method as recited in claim 20, further comprising

storing the portion of the pseudorandom sequence as elements within a storage array; and

the selecting step comprises the steps of shifting the elements of the storage array and indexing the elements of the storage array in response to the shifting.

26. (Original) The method as recited in claim 20, wherein the selecting step comprises the steps of:

identifying a most recently associated resource identifier from within the pseudorandom sequence; and

selecting a resource identifier from within the pseudorandom sequence based upon the most recently associated resource identifier.

27. (Currently Amended) The method as recited in claim 20, wherein the selecting step comprises the steps of:

determining a processor resource requirement of the instruction; and

associating the selected resource identifier with the instruction in response to the determination.

28. (Currently Amended) The method as recited in claim 20, wherein the selecting step comprises the steps of:

comparing the selected resource identifier to an allocation bound to determine whether a processor resource corresponding to the selected resource identifier is allocatable; and

associating the selected resource identifier with the instruction in response to the determination.

29. (Currently Amended) The method as recited in claim 28, further comprising the step of modifying the allocation bound in response to a deallocation of a processor resource.

30. (Currently Amended) The method as recited in claim 28, further comprising the step of generating an instruction decode stall signal in response to a determination that the processor resource corresponding to the selected resource identifier is not allocatable.

31. (Currently Amended) A system comprising:

a memory storage device;

a bus coupled to the memory storage device;

a processor coupled to the bus, comprising a resource allocator for allocating one or more processor resources to an instruction; and

the resource allocator comprising:

a sequence generator that generates one or more resource identifiers using at least a portion of a pseudorandom sequence, each resource identifier corresponding to one of the processor resources; and

a resource identifier selector coupled to the sequence generator, the resource identifier selector selecting one or more of the resource identifiers for allocation to the instruction.

32. (Original) The system as recited in claim 31, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selection circuit and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison; and

a selector coupled to the one or more comparators and the resource identifier selection circuit.

33. (Original) The system as recited in claim 31, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selection circuit and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison; and

a variable shifter coupled to the one or more comparators and the resource identifier selection circuit.

34. (Original) The system as recited in claim 31, wherein the resource identifier selector further comprises:

one or more comparators coupled to the resource identifier selection circuit and configured to compare a selected resource identifier to an allocation bound and issue a control signal in response to the comparison;

a selector coupled to the one or more comparators and the resource identifier selection circuit; and

a highest identifier allocation circuit coupled to the selector.

35. (Original) The system as recited in claim 31, wherein the sequence generator further comprises:

a logic circuit coupled to the resource identifier selector; and

a storage array coupled to the logic circuit and the resource identifier selector.

36. (Original) The system as recited in claim 31, wherein the sequence generator further comprises a storage array coupled to the resource identifier selector.

37. (Original) The system as recited in claim 31, wherein the sequence generator further comprises a logic circuit coupled to the resource identifier selector.